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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

CHOU, ALBERT T

ART UNIT PAPER NUMBER

2616

DATE MAILED: 04/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/064,332

Applicant(s)

GREENBLAT, LLIA

Examiner

Albert T. Chou

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 26 September 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-20 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 26 September 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 14-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,165,024 to Sweazey.

Note: The reference describes the operations of Node 21 in Figure 2, but it should be noted that the same operations access in each of Nodes 21-26.

Regarding claim 14, Sweazey teaches a method of controlling the transmission of messages on a ring network **[Fig. 2; Ring 20]** having a plurality of ring members **[Fig. 2; Nodes 21-26; col. 5, line 29]**, comprising:

providing a message at a first upstream ring member **[Fig. 2; Node 21]** that is available for output to a second adjacent downstream **[Fig. 2; Node 22]** ring member **[Fig. 2; When Node 21 desires to transfer data, a voucher is generated by the Voucher Generator 31 in Node 21 and placed on the ring interconnect by the Downstream Router 32 to output to Node 22; col. 6, lines 27-31];**

receiving a signal at the upstream ring member **[Fig. 2; Node 21]** from the downstream ring member **[Fig. 2; Node 22]** that indicates whether a slot is available for outputting the message on a clock cycle **[Fig. 2; Voucher Receipt Circuitry 38 in Node 22 tests whether the node is busy or not, and if not, causes Ticket Generator 39 in Node 22 to generate a ticket to the node associated with the source node; col. 6, lines 38-41, 48-50; At source node, i.e. Node 21, the Upstream Router 34 indicates to the Ticket Circuit 37 that a ticket has been return from Node 22; col. 6, lines 50-52];** and

outputting the message from the upstream ring member **[Fig. 2; Node 21]** to the downstream ring member **[Fig. 2; Node 22]** if a slot is available **[Fig. 2; The Ticket Circuit 37 in Node 21 responds by sending the information stored in the Packet Store Memory Circuitry 29 onto the ring interconnect; col. 6, lines 52-55]** and holding the message if a slot is not available **[Fig. 2; When Nodes 21 desires to transfer data, the data are stored in the Packet Storage 29 and remains there until a ticket is received at node 21; col. 6, lines 30-32, 52-55].**

Regarding claim 15, Sweazey teaches that the signal is generated based on the content of the message cycle **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source node; col. 6, lines 38-41, 48-50].**

Regarding claim 16, Sweazey teaches that the signal is generated based on whether the message will be consumed by the downstream ring member or pass through to a further downstream ring member **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source node; col. 6, lines 38-41, 48-50]**.

Regarding claim 17, Sweazey teaches that the downstream ring member is coupled to an input FIFO **[Fig. 3; A Target Buffer 56 is connected to receive information directed to that particular node; col. 8, lines 7-9]** and a through FIFO **[Fig. 3; A Cut-through Buffer 58 is a temporary repository of information not directed to that particular node; col. 8, lines 7-9]**, and the downstream ring member determines which FIFO pertains to the message **[Fig. 3; The Upstream Router 55 decodes the information and determines if it is addressed to that node; col. 8, lines 5-7]**.

Regarding claim 18, Sweazey teaches that the downstream ring member determines whether the pertinent FIFO is capable of accepting the message **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source component; col. 6, lines 38-41, 48-50]**.

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Regarding claim 19, Sweazey teaches that the message content includes at least a portion of the message type **[Fig. 2; The voucher signal includes an indication that the signal is a voucher; col. 5, lines 49-52]**.

Regarding claim 20, Sweazey teaches that the message content includes at least a portion of the message address **[Fig. 2; The voucher signal includes an identifier for the source component and an identifier for the destination component; col. 5, lines 49-52]**.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over by US Patent No. 5,165,024 to Sweazey in view of US Patent No. 6,662,256 to Foo.

Regarding claim 1, Sweazey teaches a rings-based computer system **[Fig. 2; Ring 20]** which comprises:

a plurality of ring members on a ring that communicate using point-to-point connectivity **[Fig. 2; a ring interconnection arrangement 20 comprises six individual nodes 21-26; col. 5, lines 27-29]**; a message traversing the ring from member to member **[Fig. 2; an upstream port for receiving packet information from the ring and a downstream port for placing a packet information on the ring; col. 5, lines 37-39]**; the system being adapted so that upon the message arriving at a given ring member the message is processed by that ring member if the message is applicable to that ring member **[Fig. 2; Circuits 37 responds to tickets addressed to the node; col. 6, lines 5-6, 8-9]**, and if the message is not applicable to that ring member, the message is passed on to the next ring member **[Fig. 2; If the information is not addressed to the particular destination node, it is transferred to a circuit 35 for forwarding around the ring; col. 5, lines 56-59]**; and the system being adapted so that downstream adjacent ring members provide a signal **[Fig. 2; Ticket Generator 39 to generate a ticket; col. 6, line 41]** to their upstream adjacent ring members that indicates whether a slot is available for the upstream ring member to pass the message to the downstream ring member on a given clock cycle **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source component; col. 6, lines 38-41, 48-50]**.

Sweazey does not expressly teach the rings-based computer system is on a chip basis.

Foo teaches an integrated device in computing system using the sequential bus forms a daisy chain, which interconnects each of the modules and forms a ring network within an integrated circuit device **[Fig. 3, Integrated Circuit Device 30; col. 3, lines 18-20, 62-64]**.

It would have been obvious to a person of ordinary skill in the art prior to the applicant's invention to implement the rings-based system Sweazey within an Integrated Circuit Device 30 as disclosed in Foo since each of nodes in Sweazey or modules in Foo is associated with or a part of one of the components, such as CPU, RAM, etc., within a computer system **[Sweazey: col. 5, lines 29-32; Foo: col. 1, lines 21-23]**.

The motivation for combining the reference teachings to form a rings-based system on a chip would be to reduce the number of buses or communication links, avoid the bus contention issues among connecting modules, and improve the performance of data transfer within the computer system. The motivation would have a reasonable expectation of success since both references teach that modules or components of a computer system are interconnected by forming in a ring for improving the information routing between on-chip modules.

Regarding claim 2, Sweazey teaches that the receipt of the signal indicating that a slot is not available causes the upstream ring member not to pass the message on that clock cycle **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if the component is busy, the voucher is placed in the Voucher**



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**Queue 41, which causes the upstream ring member not pass the message; col. 6, lines 31-32, 42-44].**

Regarding claim 3, Sweazey teaches that each ring member provides the signal to the immediately prior ring member each clock cycle **[The invention is capable of allowing transmission of information to be carried on concurrently between a plurality of sources and destinations; col. 6, lines 61-67].**

Regarding claim 4, Sweazey teaches that each ring member couples to the ring network by a ring interface **[Figs. 2 & 3; Node Circuitry 28; col. 5, lines 32-33]**, and the signals regarding slot availability are passed between adjacent ring interfaces **[Figs. 2 & 3; Upstream Port 43, Downstream Port 41; col. 5, lines 36-39].**

Regarding claim 5, Sweazey teaches that the ring interface includes an input FIFO **[Fig. 3; A Target Buffer 56 is connected to receive information directed to that particular node; col. 8, lines 7-9]** and a through FIFO **[Fig. 3; A Cut-through Buffer 58 is a temporary repository of information not directed to that particular node; col. 8, lines 7-9].**

Regarding claim 6, Sweazey teaches that the signal is generated by the downstream ring member **[Fig. 2; Ticket Generator 39 to generate a ticket; col. 6, line 41]** and passed to an immediately upstream ring member holding the message,

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and the signal is generated according to the FIFO for the downstream ring member that pertains to the message **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source component; col. 6, lines 38-41, 48-50]** .

Regarding claim 7, Sweazey teaches that the downstream ring member determines **[Fig. 3; The Upstream Router 55 decodes the information and determines if it is addressed to that node; col. 8, lines 5-7]** that the input FIFO pertains to the message if the message is to be consumed by the downstream ring member **[Fig. 3; A Target Buffer 56 is connected to receive information directed to that particular node; col. 8, lines 7-9]** and that the through FIFO pertains to the message if the message is not to be consumed by the downstream ring member **[Fig. 3; A Cut-through Buffer 58 is a temporary repository of information not directed to that particular node; col. 8, lines 7-9]**.

Regarding claim 8, Sweazey teaches that the signal indicates that a slot is available when the input FIFO **[Fig. 2; Circuit 35; Fig. 3; Target Buffer 56]** pertains to the message and the input FIFO can accept a message **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source component; col. 6, lines 38-41, 48-50]**.

Regarding claim 9, Sweazey teaches that the signal indicates that a slot is available when the through FIFO **[Fig. 2; Circuit 35; Fig. 3; Cut-Through Buffer 58]** pertains to the message and the through FIFO can accept a message **[Fig. 2; Voucher Receipt Circuitry 38 tests whether the node is busy or not, and if not, causes Ticket Generator 39 to generate a ticket to the node associated with the source component; col. 6, lines 38-41, 48-50]**.

Regarding claim 10, Sweazey teaches that the determination is made by the downstream ring member by examining information descriptive of the message before the message in its entirety is sent from the upstream ring member to the downstream ring member **[Fig. 2; The voucher signal includes an indication that the signal is a voucher, an identifier for the source component and an identifier for the destination component; col. 5, lines 49-52]**.

Regarding claim 11, Sweazey teaches that the information comprises data from a type field and an address field for the message **[Fig. 2; The voucher signal includes an indication that the signal is a voucher, an identifier for the source component and an identifier for the destination component; col. 5, lines 49-52]**.

Regarding claim 12, Sweazey teaches that the signal is a backpressure signal **[Fig. 2; Ticket Generator 39 to generate a ticket; col. 6, line 41]** and is generated

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based on data sent from the upstream ring member to the downstream ring member **[Fig. 2; When nodes 21 desires to transfer data, a voucher is generated by the Voucher Generator 31, placed on the ring interconnect and forwarded to the destination node; col. 6, lines 27-38]** and then back to the upstream ring member in a round trip fashion during a single clock cycle **[Fig. 2; Ticket Generator 39 to generate a ticket; col. 6, lines 41; The ticket is placed on the ring and is passed through various nodes until it returns to the node associated with the source component; col. 6, lines 48-50]**.

Regarding claim 13, Sweazey teaches that each ring member has a ring interface **[Figs. 2 & 3; Node Circuitry 28; col. 5, lines 32-33]**, and each ring interface has four interfaces **[Figs. 2 & 3; Downstream Port 41, Upstream Port 43, Receive Port 44 & Transmit Port 45; col. 5, lines 36-41]** using or providing the signal which comprises a backpressure signal **[Fig. 2; Ticket Generator 39 to generate a ticket; col. 6, line 41]**.

### ***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US Patent No. 5,590,124 to Robins discloses "Link And Discovery Protocol For A Ring Interconnect Architecture"

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- US Patent No. 5,504,747 to Sweazey discloses "Economical Payload Stream Routing In A Multiple-Ring Network"
- US Patent No. 6,266,797 to Godfrey et al. disclose "Data Transfer Network On A Computer Chip Using A Re-Configurable Path Multiple Ring Topology"
- US Patent No. 6,111,859 to Godfrey et al. disclose "Data Transfer Network On A Computer Chip Utilizing Combined Bus And Ring Topologies"
- US Patent No. 4,621,362 to Sy discloses "Routing Architecture For A Multi-Ring Local Area Network"

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Albert T. Chou whose telephone number is 571-272-6045. The examiner can normally be reached on 8:30 - 17:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on 571-272-3088. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Albert T. Chou

March 31, 2006 AC



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